REMARKS

Reconsideration of the present application is respectfully requested. Claims 2-5, 7-11, and 31-38 previously presented for examination remain in the application. Claims 5, 8, 9, 11 and 34 have been currently amended, not for prior art reasons, but to more particularly point out and distinctly claim the subject matter that applicants regard as the invention. Claims 18-21 have been canceled in this amendment to expedite allowance of the present application. Claims 1, 6 and 28-30 were previously canceled and claims 12-17 and 22-27 were previously withdrawn.

Claims 2-5, 7, 9-11, 31-32 and 35-38 are allowed.

Claims 8 and 33-34 stand objected to for informalities.

Claims 18-21 stand rejected under 35 U.S.C. § 102(b).

Claims 8 stands objected to because it is considered that it does not make sense to recite both a duty cycle correction circuit and a frequency multiplying circuit coupled to a receiving point.

Applicants have amended claim 8 to more clearly and distinctly claim the subject matter that applicants regard as the invention. In particular, applicants have clarified that the frequency multiplying circuit and duty correction circuit work together to provide a multiplied, duty-cycle-corrected output clock signal. This amendment is clearly supported by, for example, Figure 2 and the accompanying description in the specification beginning at page 5.

Claims 9 and 11 have also been amended to ensure they are consistent with the changes to claim 8.

Claim 33 stands objected to. Applicants have amended claim 33 in accordance with the Examiner's suggestion to expedite allowance of the present application.

Claim 34 stands objected to because it is considered that the phrase "an output clock signal from the duty cycle correction circuit" does not make sense and should be deleted.

Applicants were unable to locate this particular phrase in the claims. Based on applicants' best understanding of the Examiner's objection, applicants have amended claim 5 to clarify that the claimed smart buffer circuit is coupled to an output of the duty cycle correction circuit to further clarify the intended scope of claim 34.

Based on the foregoing, applicants respectfully request withdrawal of the objections to claims 8, 33 and 34.

Claims 18-21 stand rejected under 35 U.S.C. § 102(b) as being considered to be anticipated by U.S. Patent No. 5,122,679 to Ishii et al. ("Ishii"). While applicants respectfully submit that claims 18-21 as previously presented are clearly distinguished over the Ishii reference, claims 18-21 have been cancelled to expedite allowance of the present application. Thus, the rejection of claims 18-21 is moot. Applicants may pursue claims 18-21 in a separate application.

Based on the foregoing, applicants respectfully submit that the applicable rejections and objections have been overcome and claims 2-5, 7-11, and 31-38 are in condition for allowance. If the examiner disagrees or believes that further

discussion will expedite prosecution of this case, the examiner is invited to telephone applicants' representative at the number indicated below.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

Dated: November 3, 2003

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